Refine Search

Search Results -

Terms	Documents
((number or rate or total) near3 request) near10 (activity near3 bus)	4

Database:	US Pre-Grant Publication Full-Text Database US Patents Full-Text Database US OCR Full-Text Database EPO Abstracts Database JPO Abstracts Database Derwent World Patents Index IBM Technical Disclosure Bulletins	
Search:	L4	Refine Search
	Recall Text 🔷 Clear	Interrupt

Search History

DATE: Wednesday, May 09, 2007 Purge Queries Printable Copy Create Case

Set Nam side by sid		Hit Count	Set Name result set
DB=P	GPB, USPT; PLUR=YES; OP=OR		
<u>L4</u>	((number or rate or total) near3 request) near10 (activity near3 bus)	4	<u>L4</u>
<u>L3</u>	request near10 (activity near3 bus)	261	<u>L3</u>
DB=U	SPT; PLUR=YES; OP=OR		
<u>L2</u>	6073244.pn. or 5628019.pn.	2	<u>L2</u>
<u>L1</u>	6185692.pn.	1	<u>L1</u>

Freeform Search

Datab	US Pre-Grant Publication Full-Text Database US Patents Full-Text Database US OCR Full-Text Database EPO Abstracts Database JPO Abstracts Database Derwent World Patents Index IBM Technical Disclosure Bulletins	
Term	((number or rate or total) near3 request) near10 (activity near3 bus)	
Displa Gener	ay: 10 Documents in <u>Display Format</u> : - Starting with Number rate: O Hit List O Hit Count O Side by Side O Image	1
	Search Clear Interrupt	
	Search History	
DATE: W	Vednesday, May 09, 2007 Purge Queries Printable Copy Create Case	
Set Name side by side DB=PG		et Name result set
<u>L4</u>	((number or rate or total) near3 request) near10 (activity near3 bus) 4	<u>L4</u>
<u>L3</u>	request near10 (activity near3 bus) 261	<u>L3</u>
DB=USI	PT; PLUR=YES; OP=OR	
<u>L2</u>	6073244.pn. or 5628019.pn. 2	<u>L2</u>
<u>L1</u>	6185692.pn. 1	<u>L1</u>
END OF SI	EARCH HISTORY	

Refine Search

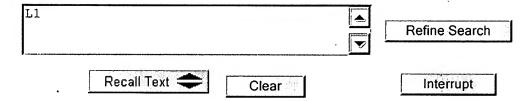
Search Results -

Terms	Documents
((variable adj1 speed) near5 bus) same (clock near3 frequency)	4

Database:

US Pre-Grant Publication Full-Text Database **US Patents Full-Text Database US OCR Full-Text Database EPO Abstracts Database** JPO Abstracts Database **Derwent World Patents Index IBM Technical Disclosure Bulletins**

Search:



Search History

DATE: Wednesday, May 09, 2007

Purge Queries

Printable Copy

Create Case

Set Name Query

Hit Count Set Name result set

side by side

DB=PGPB, USPT, USOC, EPAB, JPAB, DWPI, TDBD; PLUR=YES; OP=OR

((variable adj1 speed) near5 bus) same (clock near3 frequency) L1

<u>L1</u>

Freeform Search

Database	US Pre-Grant Publication Full-Text Database US Patents Full-Text Database US OCR Full-Text Database EPO Abstracts Database JPO Abstracts Database Derwent World Patents Index IBM Technical Disclosure Bulletins		
Term:	L3 same request		
Display: Generate	10 Documents in <u>Display Format</u> : Startine: O Hit List O Hit Count O Side by Side O Image	g with Num	ber 1
	Search Clear Interrupt	·	
	Search History		
DATE: Wedi	nesday, May 09, 2007 Purge Queries Printable Copy	Create Ca	<u>ise</u>
Set Name Que side by side DB=PGPB,	ery USPT, USOC, EPAB, JPAB, DWPI, TDBD; PLUR=YES; OP=		et Name result set
<u>L4</u> L3 s	same request	3	<u>L4</u>
` ·	r\$5 near3 speed) same bus same (clock near5 frequency)	24	<u>L3</u>
	riable adj1 speed) same bus same (clock near5 frequency)	9	<u>L2</u>
<u>L1</u> ((va	ariable adj1 speed) near5 bus) same (clock near3 frequency)	4	<u>L1</u>

Refine Search

Search Results -

Terms	Documents
(request near5 (rate or number)) same (activity near3 bus)	35

US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search:

L5		<u> </u>	Refine Search
	Recall Text 👄	Clear	Interrupt

Search History

DATE: Wednesday, May 09, 2007 Purge Queries Printable Copy Create Case

Set Name side by side		Hit Count	Set Name result set
DB=PC	GPB, USPT, USOC, EPAB, JPAB, DWPI, TDBD; PLUR = YES; OP = SPAB,	OR	
<u>L5</u>	(request near5 (rate or number)) same (activity near3 bus)	35	<u>L5</u>
<u>L4</u>	L3 same request	3	<u>L4</u>
<u>L3</u>	(var\$5 near3 speed) same bus same (clock near5 frequency)	24	<u>L3</u>
<u>L2</u>	(variable adj l speed) same bus same (clock near5 frequency)	9	<u>L2</u>
L1	((variable adi1 speed) near5 bus) same (clock near3 frequency)	4	T.1

WEST Refine Search Page 1 of 1

Refine Search

Search Results -

Terms	Documents
(361/683 361/684 361/685 361/686 322/32 709/233 370/257 710/33 710/300 710/307 710/58 710/240 710/309 710/15 710/60 710/313 712/32 340/825 713/600 713/501 713/320 713/322).ccls.	16854

US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search:

Database:

L6			Refine Search	; *** *
	Recall Text	Clear	 Interrupt	

Search History

DATE: Wednesday, May 09, 2007 Purge Queries Printable Copy Create Case

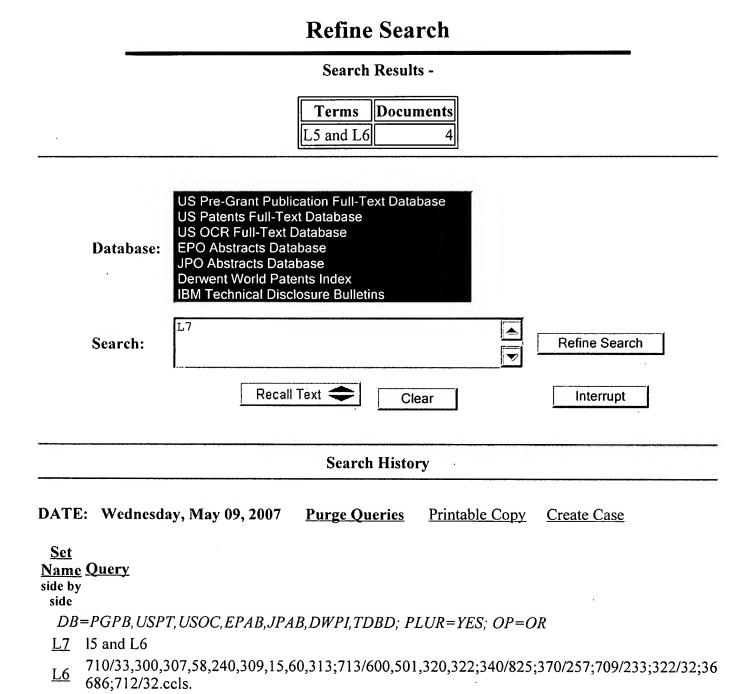
<u>Set</u>

Name Query

side by side

DB=PGPB, USPT, USOC, EPAB, JPAB, DWPI, TDBD; PLUR=YES; OP=OR

- <u>L6</u> 710/33,300,307,58,240,309,15,60,313;713/600,501,320,322;340/825;370/257;709/233;322/32;36 686;712/32.ccls.
- <u>L5</u> (request near5 (rate or number)) same (activity near3 bus)
- <u>L4</u> L3 same request
- <u>L3</u> (var\$5 near3 speed) same bus same (clock near5 frequency)
- <u>L2</u> (variable adj1 speed) same bus same (clock near5 frequency)
- <u>L1</u> ((variable adj1 speed) near5 bus) same (clock near3 frequency)



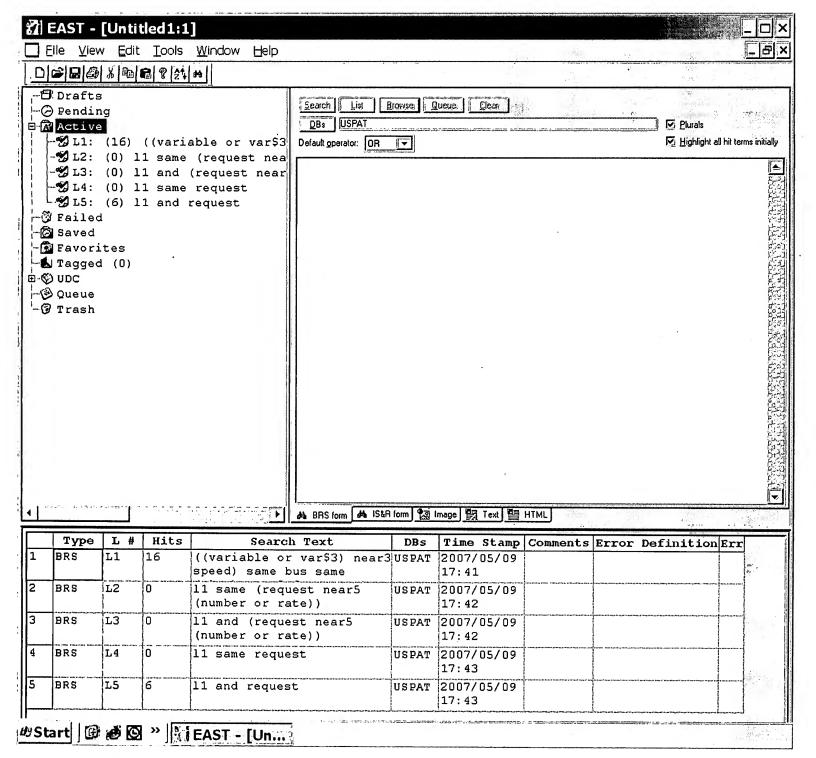
L4 L3 same request

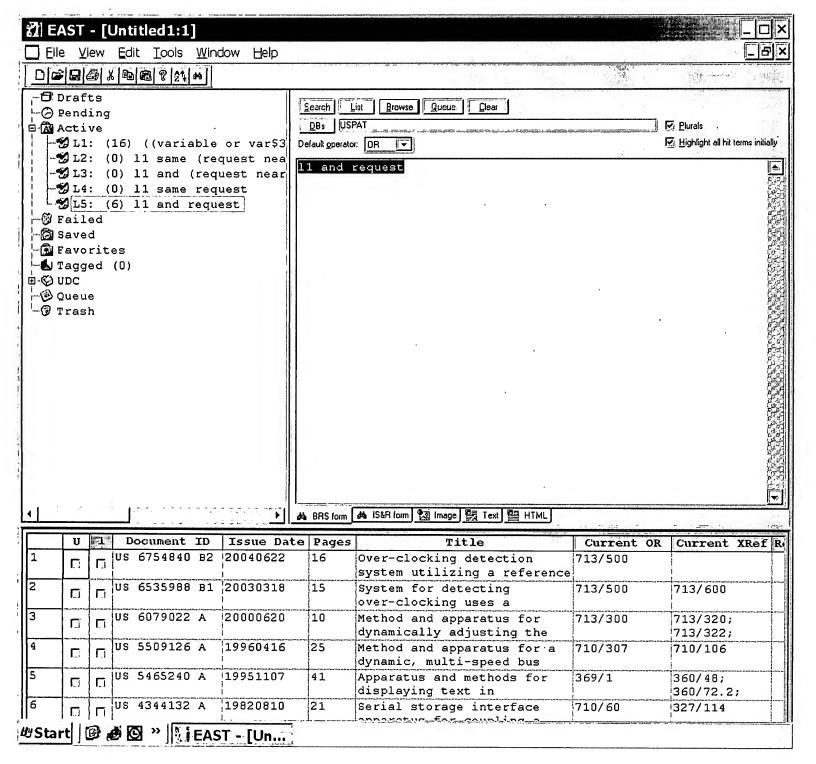
<u>L3</u> (var\$5 near3 speed) same bus same (clock near5 frequency)

<u>L5</u> (request near5 (rate or number)) same (activity near3 bus)

<u>L2</u> (variable adj1 speed) same bus same (clock near5 frequency)

<u>L1</u> ((variable adj1 speed) near5 bus) same (clock near3 frequency)







Home | Login | Logout | Access Information | Alerts |

Welcome United States Patent and Trademark Office

Sea	rch	Res	sults

BROWSE

SEARCH

IEEE XPLORE GUIDE

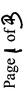
Results for "((variable and speed and bus <in>metadata) <and> (clock and frequency<in>metada" Your search matched 10 of 1566306 documents. A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.</in></and></in>			
» Search O	otions		
View Session History New Search		Modify	Search
		((variable and speed and bus <in>metadata) <and> (clock and frequency<in>metad</in></and></in>	
		□сь	eck to search only within this results set
» Key		Displa	y Format: Citation C Citation & Abstract
IEEE JNL	IEEE Journal or Magazine	view selected items Select All Deselect All	
IET JNL	IET Journal or Magazine		
IEEE CNF	IEEE Conference Proceeding	On the nature and inadequacies of transport timing delay constructs descriptions	
IET CNF	IET Conference Proceeding		Walker, P.A.; Ghosh, S.;
IEEE STD			Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction Volume 16, Issue 8, Aug. 1997 Page(s):894 - 915 Digital Object Identifier 10.1109/43.644615
			AbstractPlus References Full Text: PDF(472 KB) IEEE JNL Rights and Permissions
		□ ²	Automated bus generation for multiprocessor SoC design Kyeong Keol Ryu; Mooney, V.J., III; Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction Volume 23, Issue 11, Nov. 2004 Page(s):1531 - 1549 Digital Object Identifier 10.1109/TCAD.2004.835119
			AbstractPlus References Full Text: PDF(1144 KB) IEEE JNL Rights and Permissions
		□ 3	. /spl times/pipes Lite: a synthesis oriented design library for networks on Stergiou, S.; Angiolini, F.; Carta, S.; Raffo, L.; Bertozzi, D.; De Micheli, G.; Design, Automation and Test in Europe, 2005. Proceedings 2005 Page(s):1188 - 1193 Vol. 2 Digital Object Identifier 10.1109/DATE.2005.1
			AbstractPlus Full Text: PDF(160 KB) IEEE CNF Rights and Permissions
		<u> </u>	An accelerator for double precision floating point operations Danese, G.; De Lotto, L.; Leporati, F.; Scaricabarozzi, M.; Spelgatti, A.; Parallel, Distributed and Network-Based Processing, 2003, Proceedings, Elever Conference on 5-7 Feb. 2003 Page(s):57 - 63
			AbstractPlus Full Text: PDF(298 KB) IEEE CNF Rights and Permissions
		5	Evolution of television receivers from analog to digital van de Polder, L.J.; Parker, D.W.; Roos, J.; Proceedings of the IEEE Volume 73, Issue 4, April 1985 Page(s):599 - 612

AbstractPlus | Full Text: PDF(1560 KB) | IEEE JNL Rights and Permissions 6. A generic multielement microsystem for portable wireless applications Mason, A.; Yazdi, N.; Chavan, A.V.; Najafi, K.; Wise, K.D.; Proceedings of the IEEE Volume 86, Issue 8, Aug. 1998 Page(s):1733 - 1746 Digital Object Identifier 10.1109/5.704279 AbstractPlus | References | Full Text: PDF(364 KB) | IEEE JNL Rights and Permissions 7. A communication architecture tailored for analog VLSI artificial neural ne performance and limitations Mortara, A.; Vittoz, E.A.; Neural Networks, IEEE Transactions on Volume 5, Issue 3, May 1994 Page(s):459 - 466 Digital Object Identifier 10.1109/72.286916 AbstractPlus | Full Text: PDF(624 KB) IEEE JNL Rights and Permissions 8. A low-cost, 300-MHz, RISC CPU with attached media processor П Santhanam, S.; Baum, A.J.; Bertucci, D.; Braganza, M.; Broch, K.; Broch, T.; B Chang, E.; Kwong-Tak Chui; Dobberpuhl, D.; Donahue, P.; Grodstein, J.; Insur D.; Pearce, M.; Silveria, A.; Souydalay, D.; Spink, A.; Stepanian, R.; Varadhara Kaenel, V.R.; Wen, R.; Solid-State Circuits, IEEE Journal of Volume 33, Issue 11, Nov. 1998 Page(s):1829 - 1839 Digital Object Identifier 10.1109/4.726584 AbstractPlus | References | Full Text: PDF(208 KB) | IEEE JNL Rights and Permissions 9. Integrating communication protocol selection with hardware/software co-Knudsen, P.V.; Madsen, J.; Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction: Volume 18, Issue 8, Aug. 1999 Page(s):1077 - 1095 Digital Object Identifier 10.1109/43.775629 AbstractPlus | References | Full Text: PDF(336 KB) | IEEE JNL Rights and Permissions 10. High-Speed FPGA-Based Pulse-Height Analyzer for High Resolution X-Ra Buzzetti, S.; Capou, M.; Guazzoni, C.; Longoni, A.; Mariani, R.; Moser, S.; Nuclear Science, IEEE Transactions on Volume 52, Issue 4, Aug. 2005 Page(s):854 - 860 Digital Object Identifier 10.1109/TNS.2005.852699 AbstractPlus | Full Text: PDF(616 KB) IEEE JNL Rights and Permissions

Indexed by
Inspec

Help Contact Us Privacy & :

© Copyright 2006 IEEE -





Home | Login | Logout | Access Information | Alerts | Sitemap | Help

Welcome United States Patent and Trademark Office

BROWSE

IEEE XPLORE GUIDE

SUPPORT

◆ View Search Results | ◆ Previous Article | Next Article

SEARCH

Serrail A printer friendly

Access this document

Full Text: PDF (336 KB)

codesign

Integrating communication protocol selection with hardware/software

Download this citation

Choose Citation & Abstract

Download ASCII Text

» Learn More

Rights and Permissions » Learn More

This paper appears in: Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions Knudsen, P.V. Madsen, J. Dept. of Inf. Technol., Tech. Univ. Denmark, Lyngby, Denmark;

Volume: 18 , <u>Issue: 8</u> On page(s): 1077 - 1095

Publication Date: Aug. 1999

ISSN: 0278-0070

CODEN: ITCSDI

Digital Object Identifier: 10.1109/43.775629 INSPEC Accession Number: 6326534

Posted online: 2002-08-06 22:36:01.0

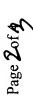
design with hardware/software partitioning is illustrated by a number of design space exploration experiments selection with hardware/software partitioning. The communication estimation model allows for fast estimation This paper explores the problem of determining the characteristics of the communication links in a computer estimation model and show, by the use of this model, the importance of integrating communication protocol but is still sufficiently detailed as to allow the designer or design tool to efficiently explore tradeoffs between buses, CPU's, ASIC's, software code size, hardware area, and component prices. A distinct feature of the communication throughput. The integration of communication protocol selection and communication driver model is the modeling of driver processing of data (packing, splitting, compression, etc.) and its impact on throughputs, bus widths, burst/nonburst transfers, operating frequencies of system components such as system as well as determining the best functional partitioning. In particular, we present a communication carried out within the LYCOS cosynthesis system, using models of the PCI and USB protocols

Index Terms

hardware-software codesign protocols Controlled Indexing

Non-controlled Indexing

system driver data processing estimation model functional partitioning hardware/software LYCOS cosynthesis PCI protocol USB protocol communication protocol computer



codesign Author Keywords Not Available

References

- 1 J. Madsen, J. Grode, P. V. Knudsen, M. E. Petersen, and A. Haxthausen, "LYCOS: The Lyngby cosynthesis system," *Design Automat. Embedded Syst.*, vol. 2, no. 2, pp. 195-235, 1997.
- D. Herrmann, J. Henkel, and R. Ernst, "An approach to the adaptation of estimated cost parameters in the COSYMA system," Proc. 3rd Int. Workshop on Hardware/Software Codesign (CODES/CASHE'94), pp.

0

Abstract | Full Text: PDF (428KB)

- J.-M. Daveau, T. B. Ismail, and A. A. Jerraya, "Synthesis of system-level communication by an allocationbased approach," Proc. 8th Int. Symp. System Synthesis, pp. 150-155, 1995. Abstract | Full Text: PDF (488KB) က
- J. Madsen and B. Hald, "An approach to interface synthesis," Proc. 8th Int. Symp. System Synthesis, pp. 16-21, 1995.

Abstract | Full Text: PDF (444KB)

- S. Narayan and D. D. Gajski, "Protocol generation for communication channels," Proc. 31th DAC, pp. 547-2
- M. Eisenring and J. Teich, "Domain-specific interface generation from dataflow specifications," Proc. 6th Int. Workshop on Hardware/Software Codesign (CODES/CASHE'98), pp. 43-47, 1998 Abstract | Full Text: PDF (72KB) 9
- G. Gogniat, M. Auguin, L. Bianco, and A. Pegatoquet, "Communication synthesis and HW/SW integration for embedded system design," *Proc. 6th Int. Workshop on Hardware/Software Codesign (CODES/CASHE'98)*, pp. 49-53, 1998.

 Abstract | Full Text: <u>PDF</u> (32KB)
- 8 J. Smith and G. De Micheli, "Automated composition of hardware components," Proc. 35th Design Automat. Conf., pp. 14-19, 1998.
 Abstract | Full Text: PDF (588KB)
- 9 J. Zhu, R. Do\"mer, and D. D. Gajski, "Syntax and semantics of the specC language," Proc. SASIMI Workshop, pp. 75-82, 1997.
- 10 A. J. Daga and W. P. Birmingham, "Interface finite-state machines: Definition, minimization, and decomposition," *IEEE Trans. Computer-Aided Design*, vol. 16, pp. 497-505, May 1997.
 <u>Abstract</u> | Full Text: <u>PDF</u> (320KB)
- 11 F. Vahid and L. Tauro, "Object-oriented communication library for hardware-software codesign," Proc. 5th Int. Workshop on Hardware/Software Codesign (CODES/CASHE'97), pp. 81-86, 1997 Abstract | Full Text: PDF (508KB)
- K. Hines and G. Borriello, "Dynamic communication models in embedded system cosimulation," Proc. 1997 34th Design Automat. Conf., pp. 395-402, 1997. CrossRef 12

- heterogeneous hardware/software systems," Design Automat. Embedded Syst., vol. 1, no. 4, pp. 357-386, D. Verkest, K. Van Rompaey, I. Bolsens, and H. De Man, "CoWare\—A design environment for
- P. Bj\win-J\wigensen and J. Madsen, "Critical path driven cosynthesis for heterogeneous target architectures," Proc. 5th Int. Workshop on Hardware/Software Codesign (CODES/CASHE'97), pp. 15-19, 4

Abstract | Full Text: PDF (400KB)

- 15 Y. Kwok and I. Ahmad, "Dynamic critical-path scheduling: An effective technique for allocating task graphs to multiprocessors," IEEE Trans. Parallel Distrib. Syst., vol. 7, no. 5, pp. 506-521, May 1993. Abstract | Full Text: PDF (1916KB)
- 16 Universial Serial Bus Specification, Revision 1.0, Jan. 1996.
- 17 1993\—Road Vehicles\—Interchange of Digital Information\—Controller Area Network (CAN) for High-Speed Communication, ISO 11898.
- 18 PCI Special Interest Group PCI Local Bus Specification, Revision 2.1, June 1995.
- 19 SCC/ESCC and ISCC Family of Products User's Manual: Zilog, Inc., 1997.
- 20 J. Garney, An analysis of throughput characteristics of universial serial bus: Media and Interconnect Technology, Intel Architecture Labs, Tech. Rep., June 1996.
- partitioning," Proc. 4th Int. Conf. on Hardware/Software Codesign (CODES/CASHE'96), pp. 85-92, 1996. P. V. Knudsen and J. Madsen, "PACE: A dynamic programming algorithm for hardware/software Abstract | Full Text: PDF (684KB)
- G. M. Amdahl, "The validity of the single processor approach to achieving large scale computing capabilities," AFIPS Conf. Proc., vol. 30, pp. 483-485, 1967. 22

Citing Documents

Scheduling with bus access optimization for distributed embedded systems, Eles, P.; Doboli, A.; Pop, P.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on

On page(s): 472-491, Volume: 8, Issue: 5, Oct 2000

Abstract | Full Text: PDF (420)

í

An architecture and compiler for scalable on-chip communication, Jian Liang; Laffely, A.; Srinivasan, S.; ~

Tessier, R.

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on

On page(s): 711-726, Volume: 12, Issue: 7, July 2004 Abstract | Full Text: PDF (1472) Scheduling and mapping in an incremental design methodology for distributed real-time embedded systems, Pop, P.; Eles, P.; Zebo Peng; Pop, T. ന

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on

On page(s): 793-811, Volume: 12, Issue: 8, Aug. 2004

Abstract | Full Text: PDF (1064)